What is claimed is:

1. A semiconductor device comprising:

a plurality of memory cells wherein each of said plurality of memory cells is connected at one of a plurality of intersections between a plurality of word lines and a plurality of bit lines;

a plurality of sense amplifiers coupled to said plurality of bit lines;

a plurality of data registers which holds date inputted from data input/output terminal;

an encoding control circuit; and

encoders to write data to said sense amplifiers based on data held in said plurality of data registers and signals outputted from said encoding control circuit.

2. The semiconductor device according to claim 1,

wherein said encoding control circuit determines a ratio of a number of data having "1" value of said data held in each said plurality of data registers.

3. The semiconductor device according to claim 2, further comprising:

a plurality of flag memory cells each one coupled to one of said plurality of word lines and

wherein said encoders invert data held in said plurality of data registers when writing to said sense amplifiers base on said signals.

4. The semiconductor device according to claim 3,

wherein said semiconductor device receives clock signals from outside of said semiconductor device,

wherein in response to Activate commands data are transferred from said memory cells to said sense amplifiers,

wherein in response to Read commands data are read from said data registers to said sense amplifiers, and are read out of the chip,

wherein in response to Write commands data are written to said data registers, and

wherein in response to a Pre-charge command, the word line is reset and said bit lines are pre-charged.

5. The semiconductor device according to claim 3,

wherein said plurality of memory cells interconnected over one of said plurality of word lines are classified into a first and second group of memory cells, and results of the classification are held in said plurality of data registers.

6. The semiconductor device according to claim 4,

wherein each of said plurality of memory cells comprises one MOS transistor and one capacitor.

7. The semiconductor device according to claim 6, further comprising:

a command decoder receiving chip select signal, row address strobe signal, column address strobe signal, and write enable signal, and

an address buffer receiving address signals.

8. The semiconductor device according to claim 3,

wherein said plurality of flag memory cells holds if the data was inverted or not when data is written to said sense amplifiers.

9. The semiconductor device according to claim 6,

wherein said data to be held in said first group of memory cells are written from said data registers to said sense amplifiers, said encoding control circuit controls so that if the number of "0" value exceeds the number of "1" in said data registers, the data will be written in said sense amplifiers as they are and "0" will be written in said flag memory cells, and if the number of "1" value exceeds the number of "0" value, the data will be inverted and written in said sense amplifiers and "1" will be written in said flag memory cells.